What is Claimed is:

1. A power-up detection apparatus, comprising:

a voltage divider for dividing an inputted power voltage in a predetermined ratio;

a potential detector for comparing a predetermined potential with a potential outputted from said voltage divider, and outputting a comparison result; and

a buffer for changing the level of said comparison result when said comparison result outputted from said potential detector is maintained at a predetermined potential for a predetermined period.

2. The apparatus of claim 1, wherein said buffer includes:

a first noise filter for changing the level of said comparison result when the comparison result outputted from said potential detector is maintained at a high level over a predetermined period; and

a second noise filter for changing the level of said comparison result when an output signal from said first noise filter is maintained at a low level over a predetermined period.

3. The apparatus of claim 2, wherein said first noise filter includes:

a delay means for delaying the comparison result outputted from said potential detector for a predetermined time; and

an operating means for logically operating said comparison result and an output signal from said delay means.

4. The apparatus of claim 3, wherein a predetermined time of said delay means is set to be longer than an interval where a predetermined noise of said external power voltage is maintained at a high level.

5. The apparatus of claim 2, wherein said second noise filter includes:

a delay means for delaying an output signal from said first noise filter for a predetermined time; and

an operating means for logically operating said comparison result and an output signal from said delay means.

6. The apparatus of claim 5, wherein a predetermined delay time of said delay means is set to be

longer than an interval where a predetermined noise of said external power voltage is maintained at a low level.

7. The apparatus of one of claims 3 to 6, wherein said delay means includes an adjustable delay line for regulating a delay time.

8. The apparatus of claim 1, wherein said buffer includes:

a first delay means for delaying the comparison result outputted from said potential detector for a predetermined time;

a first NAND gate for NANDing said comparison result and an output signal from said first delay means;

a second delay means for delaying an output signal from said first NAND gate; and

a second NAND gate for NANDing the output signal from said first NAND gate and an output signal from said second delay means.

9. The apparatus of claim 8, wherein a predetermined delay time of said first delay means is set to be longer than an interval where a predetermined noise of said external power voltage is maintained at a high

level.

10. The apparatus of claim 8, wherein a predetermined delay time of said second delay means is set to be longer than an interval where a predetermined noise of said external power voltage is maintained at a low level.

11. The apparatus of one of claims 8 to 10, wherein said delay means includes an adjustable delay line for regulating a delay time.